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KNOBBE, MARTENS, OLSEN & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ADAMS, GREGORY W	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/665,693
Filing Date: September 17, 2003
Appellant(s): AGGARWAL ET AL.

Tina Chen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 19, 2007 appealing from the Office action mailed Sept. 8, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2003/0053893	Matsunaga et al.	03-2003
6,143,083	Yonemitsu et al.	11-2000

5,810,538 Ozawa et al. 09-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al. (2003/0053893).

With respect to claim 1, Matsunaga et al. disclose a first substrate handling chamber 41, front docking port 50, robot arm 10, rear substrate handling chamber 11, buffer station 101 having a rack (Para. [0065]) configured to support a plurality of 300mm silicon wafers.

With respect to claim 2, Matsunaga et al. disclose a rack 106 configured to support a plurality of 300mm silicon wafers. Further, Applicant is respectfully reminded that claim language consisting of functional language and/or intended use phrasing is given little, if any, patentable weight as the apparatus must merely be capable of functioning, or being used, as claimed. See MPEP 2112.02, 2114. Here, Matsunaga's

rack is certainly capable of supporting 300mm wafers, either one at a time or at the same time.

With respect to claim 3, Matsunaga et al. disclose a rear substrate handling chamber 41.

With respect to claim 4, Matsunaga et al. disclose a buffer station 101 configured to create an inert environment. Further, Applicant is respectfully reminded that claim language consisting of functional language and/or intended use phrasing is given little, if any, patentable weight as the apparatus must merely be capable of functioning, or being used, as claimed. See MPEP 2112.02, 2114. Here, Matsunaga's station 101 has walls confining the interior from an environment exterior to said walls.

With respect to claim 5, Matsunaga et al. disclose a station 101 that can be selectively purged. Paras. [0064-0066].

With respect to claim 6, Matsunaga et al. disclose a z-motion capable robot arm 11. Fig. 2.

With respect to claim 7, Matsunaga et al. disclose a buffer station configured to have an internal volume less than or equal to about 18.3 liters.

With respect to claim 8, Matsunaga et al. disclose a buffer station rack configured to support twenty-five 300mm silicon wafers.

With respect to claim 9, Matsunaga et al. disclose a loadlock chamber configured to have an internal volume less than or equal to about 9.156 liters.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 & 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Yonemitsu et al. (US 6,143,083).

With respect to claims 14, Yonemitsu et al. disclose a first substrate handling chamber 100, 500, front docking port 13, 200, robot arm 66, 20, and a buffer station having a rack 40. Yonemitsu et al. further discloses different relative pitches between a front opening unified pod and a buffer station rack. C12/L22-28; C6/L63-C7/L65. It is noted that claim 14 does not recite a load lock chamber much less a load lock chamber separate from a buffer station. Yonemitsu et al. certainly disclose a load lock that can function as a buffer station. C4/L12.

With respect to claim 19, Yonemitsu et al. disclose a substrate handling chamber at standard atmosphere pressure. C7/L21-22.

With respect to claim 20, Yonemitsu et al. discloses a substrate handling chamber at reduced pressure.

With respect to claim 21, Yonemitsu et al. disclose a buffer station rack with reduced relative spacing between rack slots. C12/L22-28; C6/L63-C7/L65.

With respect to claim 22, Yonemitsu et al. disclose a buffer station rack at reduced pitch rack, accessed by robot arm. C12/L22-28; C6/L63-C7/L65.

With respect to claim 23, Yonemitsu et al. disclose a robot arm end effectors for transferring substrates. FIGS. 7-8B.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al. (2003/0053893) in view of Ozawa et al. (US 5,810,538).

With respect to claims 10 & 14, Matsunaga et al. discloses a first substrate handling chamber 12, front docking port 50, robot arm 10, rear substrate handling chamber 41, buffer station 101 having a rack (Para. [0065]), and does not disclose a buffer station rack having a reduced pitch relative to FOUP shelves. Ozawa et al. discloses a reduced pitch between a rack 18 and FOUP rack (C4/L45-53) allows multiple wafers from smaller cassettes to be placed in a single wafer boat allowing increase wafer production during one boat cycle-through. C2/L45-65. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Matsunaga et al. to include a buffer station rack having a reduced pitch relative to FOUP shelves, as per the teachings of Ozawa et al., to reduce boat cycle-through times.

With respect to claim 11, Matsunaga et al. does not disclose a robot arm configured to employ a variable pitch end effector. Ozawa et al. discloses a variable pitch end effector (C4/L45-53) that allows multiple wafers from smaller cassettes to be placed in a single wafer boat allowing increase wafer production during one boat cycle-through. C2/L45-65. Therefore, it would have been obvious to one having ordinary skill

in the art at the time the invention was made to modify the apparatus of Matsunaga et al. to include a variable pitch end effector, as per the teachings of Ozawa et al., to reduce boat cycle-through times.

With respect to claims 12-13, Matsunaga et al. disclose a first substrate handling chamber 12 configured to operate at atmospheric pressure and at a reduced pressure.

With respect to claim 15, Matsunaga et al. disclose a loadlock chamber 21, 31 having a loadlock rack (Para. [0022], L3-4).

With respect to claim 16, Matsunaga et al. disclose a rear substrate handling chamber 41.

With respect to claim 17, Matsunaga et al. disclose a loadlock capacity of 1 to 7 substrates.

With respect to claim 18, Matsunaga et al. disclose a rack 106 configured to support a plurality of 300mm silicon wafers.

(10) Response to Argument

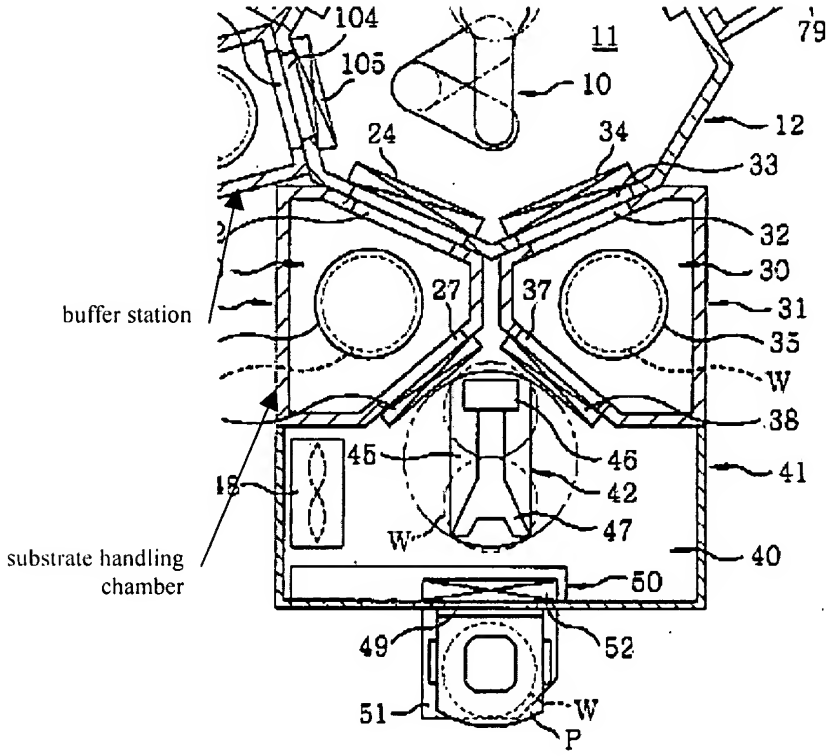
Rejection of Claims 1-9 by Matsunaga et al. (US 2003/0053893).

Instant Application	Matsunaga et al. (US 2003/0053893)
Claims 1-9	
1st substrate handling chamber	FIG. 5: 41
front docking port on outside surface of 1st substrate handling chamber	FIG. 5: 50-52
robot arm in 1st substrate handling chamber	FIG. 5: 42

loadlock chamber joined to 1st substrate handling chamber	FIG. 5: 20, 30
buffer station adjacent to 1st substrate handling chamber and separate from loadlock chamber	FIG. 5: 101 where adjacent is interpreted as close to, but not required to be connected to.
buffer station rack/shelves	79 (Para. [0065])

Matsunaga et al. disclose each and every limitation in claims 1-9. Appellant argues that the cited prior art does not disclose a buffer station adjacent a first substrate handling chamber. The language in claim 1 distinguishes adjacent to (or close in proximity) from connected to (or attached). For example, Appellant defines a front docking port as "**located on** an outside surface" (line 3, Emphasis added) which contrasts with a buffer station which is "**adjacent to** the first substrate handling chamber" (line 7, Emphasis added). Clearly the front docking port is touching and the buffer station is not. Moreover, Appellant does not define "adjacent" within the specification, and adjacent has a well established meaning of objects that are in close proximity to each other but not inherently touching.

Thus, claim 1 locates the buffer station close to but not connected with a substrate handling chamber. As shown in the claim chart above and in FIG. 5 reproduced below Matsunaga's front docking port 50, 52 is clearly located on an outside surface of a first substrate handling chamber 41 via walls that touch. Matsunaga's front docking port comprises walls that connect the substrate handling chamber walls.



Matsunaga's front docking port allows a wafer cassette to be placed on cassette port plate 51 such that arm 42 can reaches wafers W. Matsunaga's structure 50-52 is a docking port and is located on an outside surface of a first substrate handling chamber 41. And Matsunaga's buffer station 101 is clearly adjacent to Matsunaga's handling chamber insomuch as it is literally touching the wall of substrate handling chamber 41. With respect to claims 2-9 Appellant argues for allowable based on the claim 1 arguments which have been addressed. Thus, Matsunaga disclose each and every limitation of claims 1-9.

Rejection of claims 14 & 19-23 over Yonemitsu et al. (US 6,143,083).

Instant Application	Yonemitsu et al. (US 6,143,083)
Claims 14 & 19-23	

a substrate handling chamber	FIG. 11: 100
front docking port on outside surface of a substrate handling chamber, capable of mating with a cassette	FIG. 11: 13; C16/L40.
cassette rack	C16/L40
robot arm in a substrate handling chamber	20, 24
buffer station adjacent to a substrate handling chamber and separate from loadlock chamber	FIG. 11: 30; C4/l12
buffer station rack/shelves	FIG. 11: 40

Yonemitsu et al. disclose each and every limitation in claims 14 & 19-23. Specifically, one of Yonemitsu's structures labeled 30 is a buffer. Yonemitsu discloses that an intermediate substrate holding chamber 30 where intermediate is interpreted as a holding place for wafers in transit between two locations.

Yonemitsu further disclose a buffer chamber 40 that "can function as a load-lock chamber when a substrate is transferred between the atmospheric pressure section and the substrate transfer chamber maintained under reduced pressure." C4/L13. But this requires it to be one or the other but not both a buffer and load lock at the same time. Yonemitsu discloses the ability for buffer 40 to operate as a holding place for substrates in transit, separate from a load lock, a function clearly reserved for lower handling

chamber 40. Yonemitsu's loadlock 300 is clearly on a substrate handling chamber 100, 500 because they share a common wall (indicated generally as 50 & 54 in FIG. 4). Further, buffer 40 is adjacent a first substrate handling chamber because it is at least next to chamber 500 and connects to chamber 500 through gate valve 92. Were it not adjacent, gate valves 92 would be irrelevant.

Moreover, the front docking port 100 is certainly on an outside of substrate handling chamber 500 as they share a common wall and allow cassettes to be input through opening 13 and docked at load lock 200.

Applicant next argues that Yonemitsu's buffer is not purgeable, arguing that "purgeable" only requires gas to expel contaminants. Whether purgeable requires an input of gas to expel contaminants is irrelevant because Yonemitsu discloses an enclosed body with sealing doors 91, 92 that is evacuated (C5/L49) with input of an atmospheric gas. C5/L51. Thus, Yonemitsu et al. disclose each and every limitation of claims 14 & 19-23.

Rejection of claims 10-18 over Matsunaga in view of Ozawa et al. (US 5,810,538).

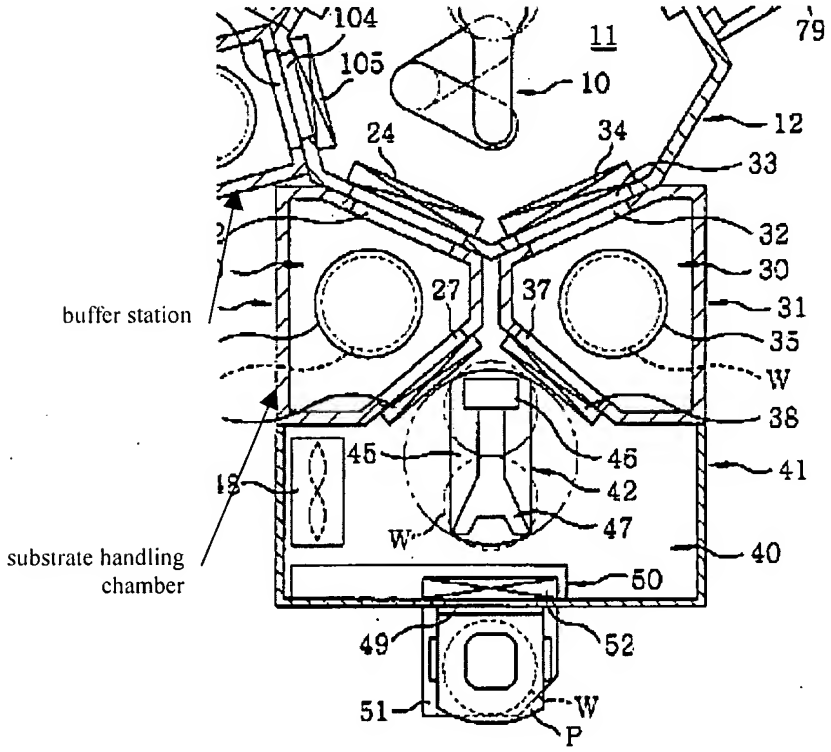
Instant Application	Matsunaga et al. (US 2003/0053893)
Claims 10-18	
1st substrate handling chamber	FIG. 5: 41
front docking port on outside surface of 1st substrate handling chamber	FIG. 5: 50-52
robot arm in 1st substrate handling chamber	FIG. 5: 42
loadlock chamber joined to 1st	FIG. 5: 20, 30

substrate handling chamber	
buffer station adjacent to 1st substrate handling chamber and separate from loadlock chamber	FIG.5: 101
buffer station rack/shelves	FIG. 5: 79 (Para. [0065])
	Ozawa et al. (US 5,810,538)
reduced pitch	a reduced pitch between a rack 18 and FOUP rack (C4/L45-53)

Matsunaga et al. disclose each and every limitation in claims 1-9. Appellant argues that the cited prior art does not disclose a buffer station adjacent a first substrate handling chamber. The language in claim 1 distinguishes adjacent to (or close in proximity) from connected to (or attached). For example, Appellant defines a front docking port as "**located on** an outside surface" (line 3, Emphasis added) which contrasts with a buffer station which is "**adjacent to** the first substrate handling chamber" (line 7, Emphasis added). Clearly the front docking port is touching and the buffer station is not. Moreover, Appellant does not define "adjacent" within the specification, and adjacent has a well established meaning of objects that are in close proximity to each other but not inherently touching.

Thus, claim 1 locates the buffer station close to but not connected with a substrate handling chamber. As shown in the claim chart above and in FIG. 5 reproduced below Matsunaga's front docking port 50, 52 is clearly located on an outside

surface of a first substrate handling chamber 41 via walls that touch. Matsunaga's front docking port comprises walls that connect the substrate handling chamber walls.



Matsunaga's front docking port allows a wafer cassette to be placed on cassette port plate 51 such that arm 42 can reaches wafers W. Matsunaga's structure 50-52 is a docking port and is located on an outside surface of a first substrate handling chamber 41. And Matsunaga's buffer station 101 is clearly adjacent to Matsunaga's handling chamber insomuch as it is literally touching the wall of substrate handling chamber 41. With respect to claims 2-9 Appellant argues for allowable based on the claim 1 arguments which have been addressed.

Appellants argues that Ozawa does not disclose "a first substrate handling chamber, a front docking port located on the outside surface of the first substrate

handling chamber, a robot arm located in the first substrate handling chamber, a loadlock chamber joined to the first substrate handling chamber, and a buffer station adjacent the first substrate handling chamber and separate from the loadlock chamber, the buffer station being purged with an inert internal environment separate from the first substrate handling chamber, the buffer station having a rack defining multiple shelves for holding substrates, wherein the shelves of the buffer station rack have a reduced pitch relative to shelves of a front opening unified pod (FOUP) for the same size substrates" as required in claim 10 are irrelevant because Matsunaga discloses each and every limitation as shown above.

Appellant argues that there is no suggestion to combine the references because "nothing in Ozawa suggests or indicates that a reduced pitch buffer station would reduce boat cycle-through times. Ozawa et al. discloses in column 2,lies 45-65 that a reduced pitch between a rack 18 and FOUP rack (C4/L45-53) allows multiple wafers from smaller cassettes to be placed in a single wafer boat allowing increase wafer production during one boat cycle-through.

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Ozawa recognizes that pitch differences between a wafer cassette, i.e. FOUP, and buffer 18 are inherent in the industry and solves this problem by modifying a transport arm 23 that changes pitch between said FOUP and buffer "to match the difference of a

wafer accommodating pitch of the wafer cassette and a wafer accommodating pitch of the [buffer] 18". C4/L47. Finally, Ozawa is analogous art for at least the reason that it discloses a wafer processing apparatus similar to Matsunaga's. And, Ozawa's ultimate goal is to solve the problem of increasing cycle times (C2/L45-65) by reducing cassette placement operations (C2/L67) despite the fact that buffer stations 18 have a reduce pitch relate to FOUP shelves. Thus, Ozawa is a modifying reference with combined with Matsunaga's wafer handling apparatus. Matsunaga in view of Ozawa disclose each and every claim limitation recited in claims 11-18.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Gregory W. Adams, Examiner AU 3652

Conferees:

Saul Rodriguez, SPE AU 3652

Meredith Petravick, Appeals Specialist TC 3600

SAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER